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## **DESIGNING FOR TESTABILITY GUIDELINES**

Testing of surface mount assemblies is much more critical than conventional through-hole assemblies for several reasons:

- Passive components are smaller in size and leadless.
- Many packages now have a large number of leads on 25 mil. vs. 50 - 100 mil. centers.
- The increased component densities result in tighter spacing and dual sided mountings.
- Lack of test access; through-hole assemblies automatically provide test access on the solder side of the board.

This is why testability must be considered at the early stages of product development (while the board is being designed not after the design is complete!).

The purpose of these guidelines is to provide the designer with information that will allow the use of bed-of-nails testing techniques for surface mount circuits. The goal is to provide a minimal set of rules that will ensure testability and that is independent of test method, be it Functional or In-Circuit. Furthermore, the guidelines are intended to be generic and non-vendor specific.

The SMTA Testability Committee has devised a set of guidelines for the designer that, when followed properly, will ensure testability. Deviation from these guidelines will not prevent testing, but it will invariably:

- increase the time for troubleshooting (slower through-put)
- offer less reliable probing
- reduce test yields
- force alternate or less desirable test methods to be used

The final result will be higher production cost and lower overall profit since these added costs cannot be passed on to the customer.

This document is excerpted from the *Designing For Testability Handbook* published by the SMTA Testability Committee. All comments and feedback on these guidelines should be mailed to: SMTA Testability Committee, P.O. Box 1811, Los Gatos CA 95031.

## **MECHANICAL GUIDELINES**

The first guideline impacts the probability that the spring-loaded probes will reliably contact the Device Under Test (DUT). The criteria used in the tolerance analysis were a single point (spear head) probe, the worst-case tolerance internal to the probes and their mounting, tolerances associated with DUT platen (probe plate) alignment, and test pad diameter.

Also, statistical analysis of the number of contact misses was not considered, since a contact failure on any test caused by improper tolerances is not considered acceptable and invalidates the test.

With larger PC boards, these tolerances become more difficult to control than with smaller boards. The tolerance build-up directly and adversely impacts the test pad size. Larger diameter test pads may be required for the same probe contact reliability as the board size increases.

### **A. Provide Accurate Tooling Holes.**

- A. Tolerance from the DUT Datum to the test pad should be  $\pm 0.002$ " (0.05mm).

Tooling pin location is critical and every effort should be made to reduce the indexing tolerance. In cases where PC boards are manufactured in panels and the broken out, datum holes should be supplied both in the mother panel and in each individual board. The datum holes (at least two) in the panels are required for accurate processing and for subsequent testing and possible rework. If necessary because of space considerations, breakaway tabs can be used to carry the datum holes for the assembly process and testing the DUT. The same datum holes must be used to fabricate, populate, and test the PC board to ensure probing accuracy.

2. Place two tooling holes on the DUT as far apart as possible with a tolerance between holes of  $\pm 0.002$ " (0.05mm).

The tooling holes should be diagonally opposite for the best probing accuracy and must be part of the primary drilling operation. The tooling holes must not be indexed from the edge of the board, as board profile tolerances are generally not controllable enough for an accurate datum.

The tooling holes should accept at least 0.125" (3.1mm) diameter pins to maintain stability and alignment of the board with the fixture. If dual sided probing is required, the tooling pins may have to be long enough to go through both fixture plates.

3. Tolerance of tooling hole diameters should be  $+0.003"/-0.000"$  ( $+0.08/-0.00\text{mm}$ ).

Non-plated tooling holes are preferred as they decrease the likelihood of solder build-up and make the  $+0.003$  tolerance more feasible. The diameter of plated through holes is very difficult to control.

### DUT Required Tolerances

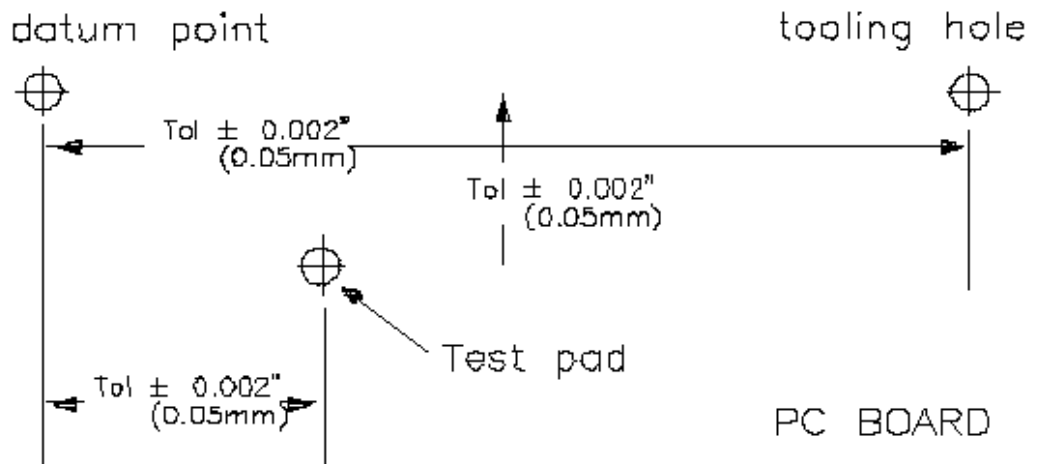


Figure 1 shows the tooling tolerances.

**B. Probe Pads should be .035/.040" (.89/1.0mm) diameter.**

Using the tolerances in guideline #1, this is the minimum pad diameter that will guarantee probe contact. Test pad size is dependent on many factors, such as accuracy of tooling, and PC manufacturing processes, as well as the physical size of the board.

For small probes, the 0.035" (1.0mm) pad size should be used, and for the larger probes, the 0.040" (0.9mm) size. It is feasible to use smaller (0.025"/0.61mm) test pads on small boards (under 12" square) but the designer should check fixture cost and tolerance specifications.

Figure 2 shows the minimum desirable pad-to-pad tolerances.

### Minimum Desirable Test Pad Positioning

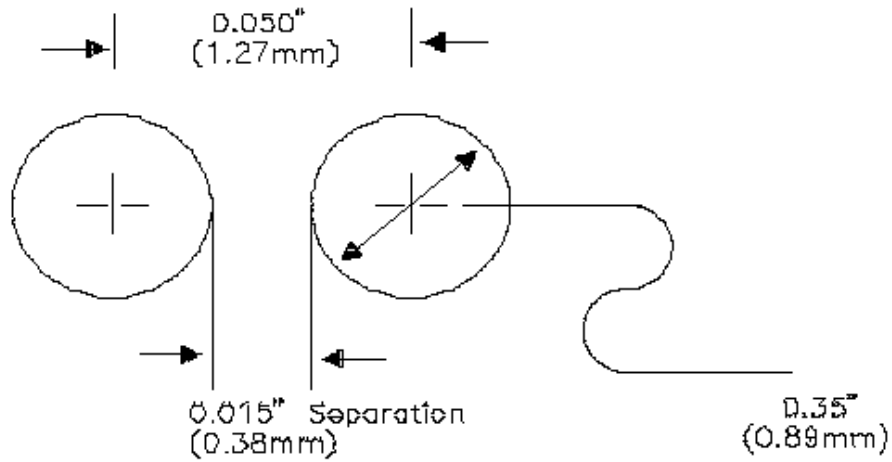


Figure 2

**C. Component height on probed side of DUT should not exceed .250" (6.4mm).**

Tall components on the probe side of the board will require cutouts or relief in the platen. They can be accommodated, but the cost of special machining of the platen and loss of platen strength should be considered. Excavation of the platen also restricts test probe placement.

When necessary, test pads should be placed 0.2" (5.0) away from tall components (greater than 0.2" high) to allow for milling tolerances. See Figure 3.

Diagram Showing Free Area Around Test Pad For Components Greater Than 0.250" In Height

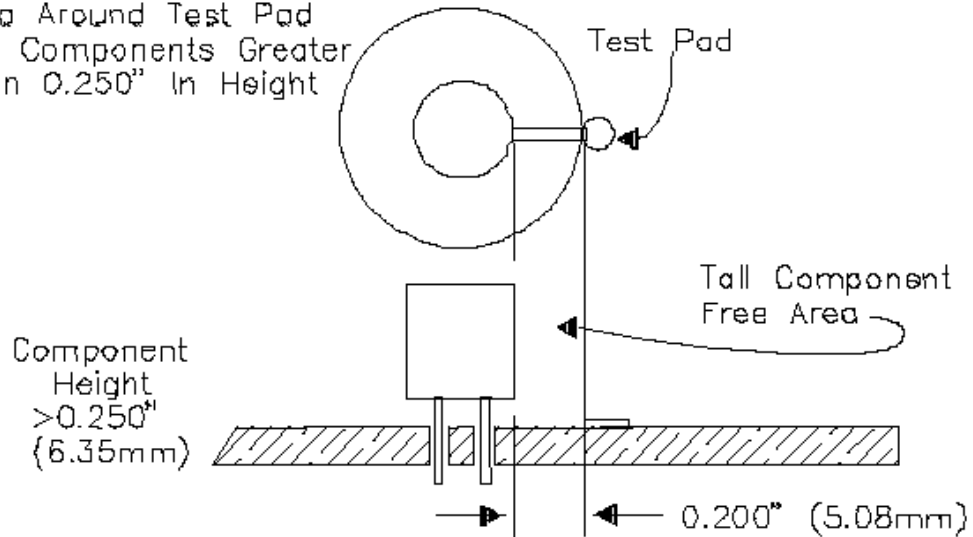


Figure 3

**D. There must be a free area with no components or test pads within .125" (3.2mm) of DUT edges.**

This requirement can be recognized easily if consideration is given as to how the DUT will be handled in the test fixture and in storage. This ensures that components will not interfere with the vacuum seal and seating of the probe. It also provides longer life for the gasket. Some fixtures, especially those designed for double-sided testing, require clear edges for mounting/sealing to the PC board. Robotic or pick and place handling systems may also require accessible edges.

- E. A 0.018" (0.46mm) annulus, free of components or other obstructions, must be left around each test pad.**

This is to prevent shorting components or test pads when a worst-case tolerance situation exists and probe heads other than single point are used. It assumes that no component within 0.2" (5.1mm) of the test pad exceeds 0.250" (6.4mm) in height. Further, when a high component is within 0.2" (5.1mm) of the pad, space for mounting the probe receptacle in the fixture must be provided. See Figure 4.

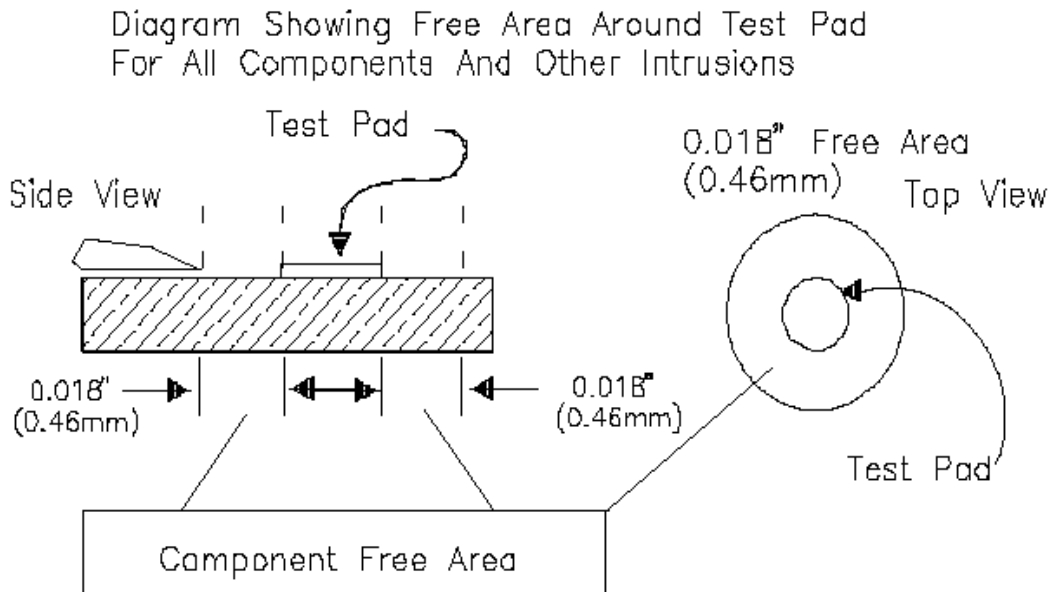


Figure 4

- F. Edge of test pads on component side must have a minimum 0.040" (1.0mm) clearance from components.**

This is to avoid striking the component, which may cause probe or component damage.

- G. All surfaces to be probed must be solder-coated, or coated with an equivalent conductive, non-oxidizing surface.**

Solder has proven to be an excellent material to probe. Solder oxides are soft and easily penetrated providing good probe contact while helping to retain probe tip sharpness. It is imperative to keep the surface to be probed clean to provide reliable contact.

- H. Test Pads must not be covered by solder resist or legend ink.**

If the resist or ink covers part of the test pad, the area available for contact will be reduced. It should also be noted that using a probe with a large contact head, such as a serrated or crown, might interfere with pad contact (see figures 5A and 5B).

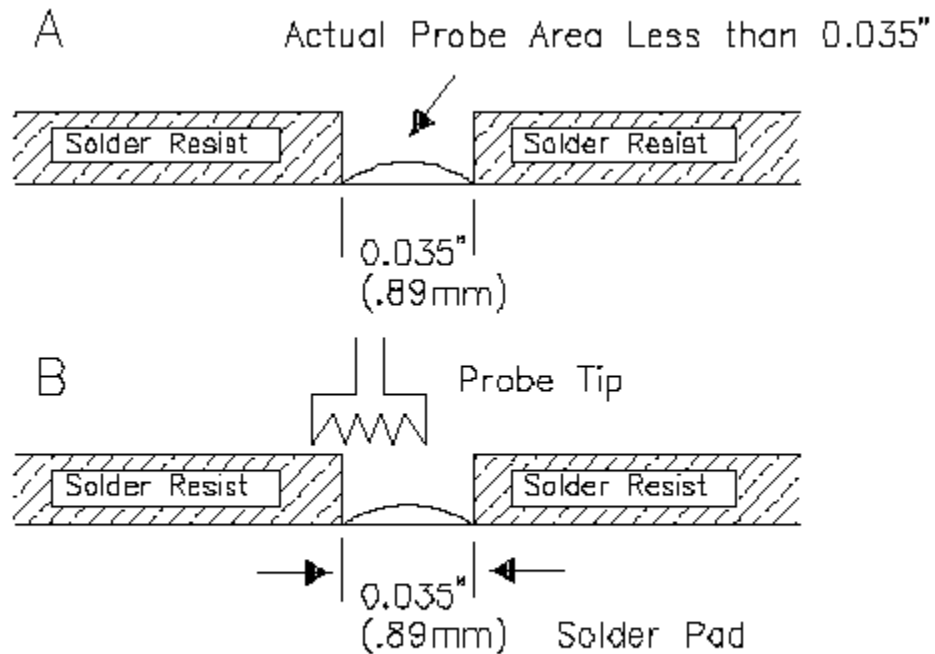


Figure 5

**I. All through holes should be filled.**

Filling all the holes reduces fixture air leakage and prevents spear point probes from sticking in unfilled holes (vias). Unfilled holes also contribute to intermittent probe contact. When air is pulled through unfilled vias, the probes may become contaminated causing intermittent contact.

Unfilled holes may require the use of a rubber mat or other means to cover the assembly during test. This is to ensure a proper vacuum seal and fixture operation. The mat may preclude probing the board under test for fixture verification or for debugging tests.

Where reflow soldering is used and space permits, the vias should be tented over with soldermask (dry film). Separate dedicated, solder coated test pads should then be provided.

**J. A 0.125" (3.2mm) annular area around tooling holes must be clear of components and test pads.**

This prevents damage to components when placing and removing the board from the test fixture. Many tooling holes are stepped for positioning the height of the DUT. The danger of shorting component leads exists even with un-stepped pins.

**K. Probe should contact Test Pads or vias, not components or component leads of surface mount components.**

Contact pressure can cause an open or make a cold solder joint appear good. Component mounting variations may also result in missing the target, probe glancing causing fixture induced shorts, and probe damage.

- L. Avoid probing both sides of the PCBA. Use vias to bring Test Pads to one side (preferably the non-component side of the board).**

It is always preferable to design a PC board so that testing can be accomplished from the preferred non-component side. This allows the use of simpler, less expensive, more reliable fixtures. Troubleshooting with double-sided fixturing is very limited and more difficult.

- M. Test Pads should be 0.100" (2.54mm) apart (center spacing) if possible, in preference to 0.05" (1.27mm) spacing.**

Wider center spacing of test pads allows the use of less costly and more reliable probes. Also drilling and wiring the fixtures will be less expensive. Smaller probes for 0.050" (1.27mm) spacing are less reliable, fragile, and easily damaged.

- N. Provide test pads for unused logic pins.**

Unused pins that have logic associated with them should have accessible test pads for short tests and future ECO implementation.

- O. Provide alternate test pads for each net whenever possible.**

It is important to have alternate probe locations for electrical nets to enable fixture modifications for ECO implementation.

## **ELECTRICAL DESIGN GUIDELINES**

In addition to the mechanical rules stated above, increased testability can be gained by incorporating some simple electrical guidelines.

The following three guidelines are generic to most In-Circuit testers on the market today. These guidelines will aid greatly in improving test coverage and reliability while reducing test cost.

### **A. Test Pads must be provided for all electrical nodes.**

A node is defined as an electrical connection between two or more components either analog or digital. Unused pins of ICs, connectors, etc. are included. Test pads should be provided for all I/Os, power, ground and return signals.

Each IC should also have a test pad on the power and ground nodes as close as possible to the device. For devices having more than one power or ground pin, additional test pads should be added. As a rule, a power and ground test pad should be provided within 1" (2.54mm) of each IC. Fixturing for testers in the 5 MHz and above test speeds will require power pins to be placed on each IC for good power supply coupling.

**NOTE:** Jumpers (zero ohm resistors), fuses, and SPST switches are treated as two lead components and are connected between two electrical nodes; therefore, each node requires a separate test pad.

### **B. Do not rely on edge connectors or circuit traces as test points.**

Probing an edge connector plating or circuit trace may produce poor contact reliability. Gold plated fingers are also easily damaged with test probes. A better approach is to use a dedicated soldered test pad. Conductor traces can be expanded to 40-mil width if direct probing of the trace is desired.

### **C. Distribute Test Points evenly over PC board.**

When the probes are not evenly distributed on the platen or concentrated in one area, the resulting high stresses may bow the DUT or platen. This may cause some probes not to make contact with the test pads and can also result in vacuum sealing problems or possible board damage. It is recommended that the probes be distributed about the board as much as possible.

**D. Do not wire IC control lines directly to Ground, VCC, or a common resistor.**

With CPUs, there are at least three key types of pins that should be considered: external instruction access pins, initialize pins, and output enable pins.

In the example (figure 6), the External Access (EA) feature of the 8048 has been grounded making it impossible to use the library test routine. This may force specialized testing or reduced coverage.

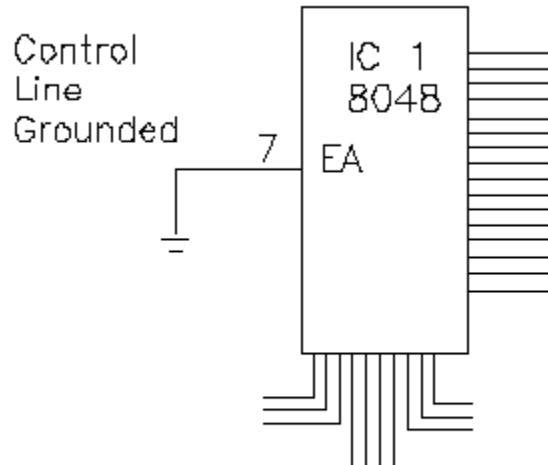


Figure 6

Similarly, control lines that are tied to a common resistor cannot be toggled independently to initialize the circuit (see figures 7, 8, and 9). Use individual pull-down or pull-up resistors.

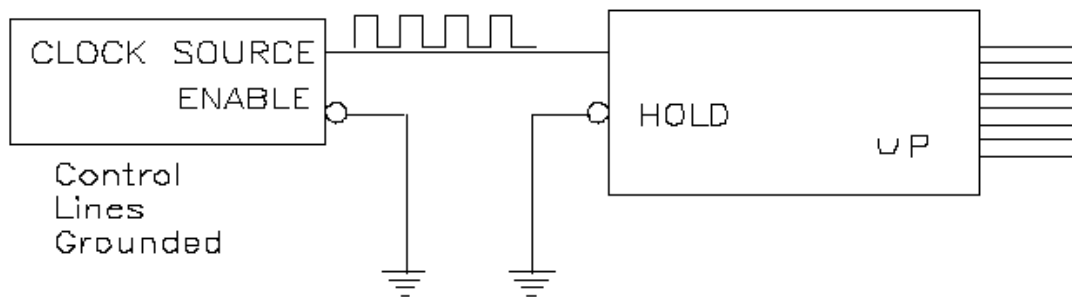


Figure 7

down or pull-up resistors.

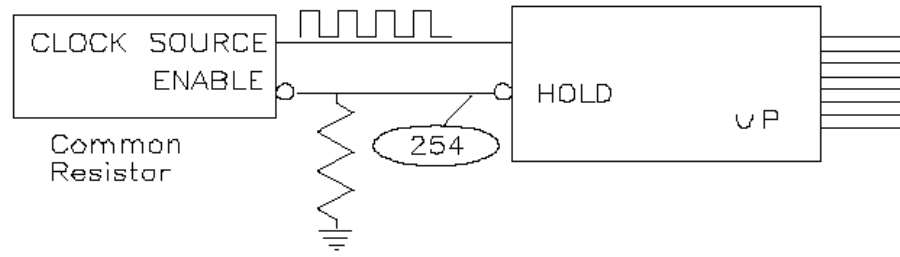


Figure 8

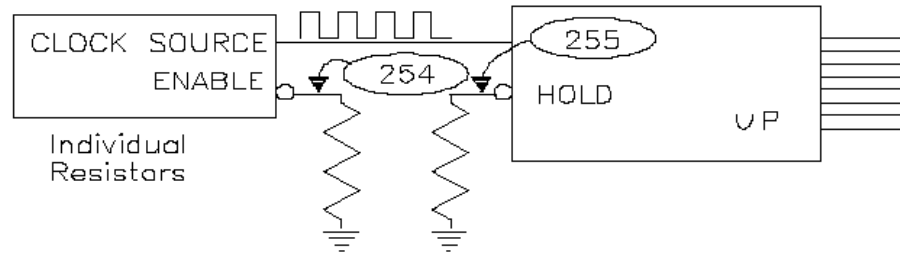


Figure 9

**E. Clock sources must be controllable by the ATE Test equipment.**

A running clock on the board will cause an unstable test. Disabling can be accomplished by means of jumpers or tri-state buffers.

**F. Power-On Reset circuits must be backdrivable.**

The RC circuits for power-on reset should be isolated from other digital components with a digital buffer. Three simple ways to provide a backdrivable-reset signal are shown in figure 10. Figures 11, 12, and 13 illustrate possible uses in reset circuitry.

Three simple backdrivable constant low sources to allow control are:

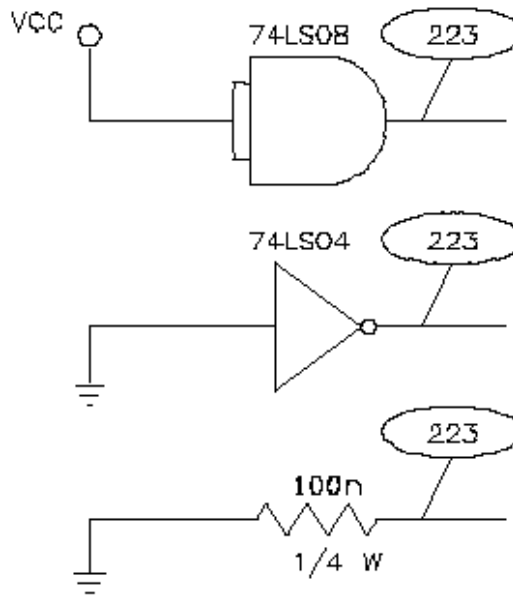


Figure 10

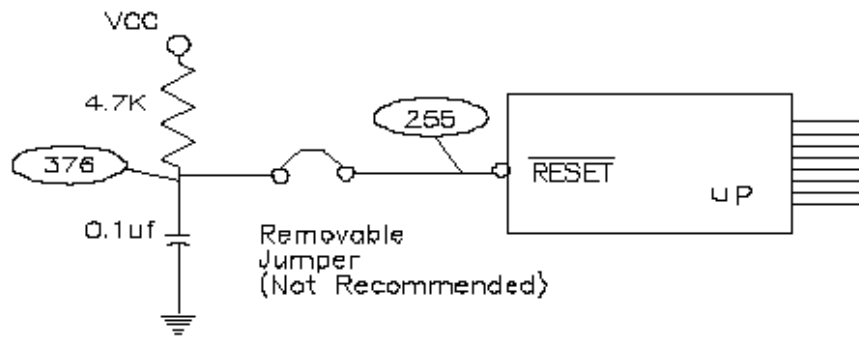


Figure 11

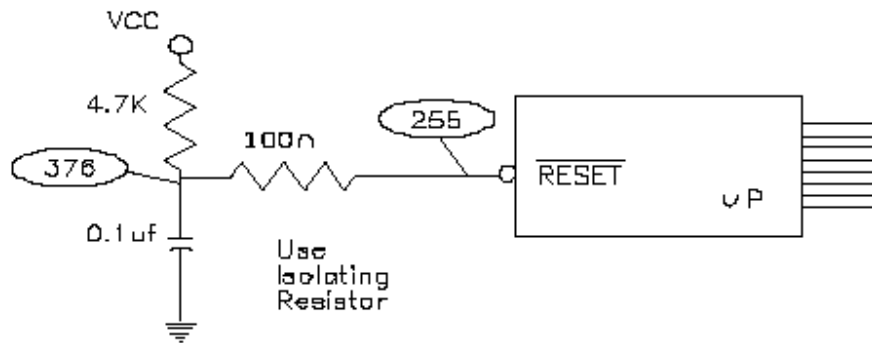


Figure 12

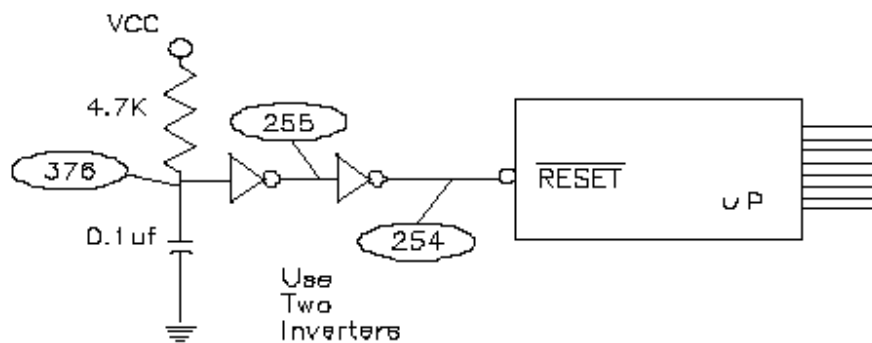


Figure 13

**G. Move Test Pads only when absolutely necessary.**

Provided only a few test pads have to be moved when there is a design change, it may be possible to modify the test fixture rather than replace it. This can be accomplished by using a bare PC board as a drill guide. As long as the new location of the pad is at least 0.1" from the old location, drilling the new hole will not cause a break-through into the wall of the old hole.

**H. Provide a Test Pad on the power and ground nodes as close as possible to the device.**

Each IC should have a test pad on the power and ground nodes as close as possible to the device to minimize voltage drops and noise problems. For devices having more than one power and ground pin, additional pads should be provided. Designers should also ensure there is adequate decoupling for ICs to reduce noise spikes.

**I. PAL circuits should have an initialization or reset pin.**

In order to have higher test coverage on PAL circuits, an initialization step is required in the design of the PAL. This will set the outputs of the PAL to a known state prior to actual test.

**J. Use tri-stateable ICs in circuit designs when possible.**

In order to prevent excessive back driving of output pins during ICT testing, it is recommended to use tri-stateable IC's in circuit designs. This guideline is mainly recommended in bus-oriented designs.